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PLEASE NOTE: YOU MUST COMPLETE THE FOLLOWING

COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT AND DESIGN APPLICATIONS

As a below named inventor, I hereby declare that· my residence, post office address and citizenship are as stated next to my name; that I verily believe that I am the original, first and sole inventor (if only one inventor is named below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled.

Insert Title: ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT

Fill in Appropriate Information - For Use Without Specification Attached:

the specification of which is attached hereto If not attached hereto,
the specification was filed on _____ as
United States Application Number _____,
and amended on _____ (if applicable) and/or
the specification was filed on _____ as PCT
International Application Number _____; and was
amended under PCT Article 19 on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1 56.

I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representative or assigns more than twelve months (six months for designs) prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as follows.

I hereby claim foreign priority benefits under Title 35, United States Code, §119(a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed

Insert Priority Information: (if appropriate)

Prior Foreign Application(s)			Priority Claimed	
87294/2000 (Number)	KOREA (Country)	December 30, 2000 (Month/Day/Year Filed)	☒ Yes	☐ No
(Number)	(Country)	(Month/Day/Year Filed)	☐ Yes	☐ No
(Number)	(Country)	(Month/Day/Year Filed)	☐ Yes	☐ No
(Number)	(Country)	(Month/Day/Year Filed)	☐ Yes	☐ No

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional applications(s) listed below

Insert Provisional Application(s): (if any)

(Application Number)	(Filing Date)
(Application Number)	(Filing Date)

All Foreign Applications, if any, for any Patent or Inventor's Certificate Filed More than 12 Months (6 Months for Designs) Prior to the Filing Date of This Application:

Insert Requested Information: (if appropriate)

Country	Application Number	Date of Filing (Month/Day/Year)

I hereby claim the benefit under Title 35, United States Code, §120 of any United States and/or PCT application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States and/or PCT application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to the patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

Insert Prior U.S. Application(s): (if any)

(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)
(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)

I hereby appoint the practitioners at **CUSTOMER NO. 2292** as my attorneys or agents to prosecute this application and/or an international application based on this application and to transact all business in the United States Patent and Trademark Office connected therewith and in connection with the resulting patent based on instructions received from the entity who first sent the application papers to the practitioners, unless the inventor(s) or assignee provides said practitioners with a written notice to the contrary:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of First or Sole Inventor: Insert Name of Inventor → Insert Date This Document is Signed

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built-in voltage of a PN junction, since the diodes are connected to each other in a forward direction. As is well known in the art the built-in voltage of the PN junction may vary.

[0028] Yet, as the present diodes are connected in series, a voltage of the node A is dropped down by an amount (number of diodes Dn x 0.7V) so as to be applied to the substrate. For instance, if 5 diodes are connected in series to each other, a voltage at a node B becomes the voltage attained by subtracting 3.5V from the voltage at node A. Once the voltage over 3.5V is applied to the pad, all the diodes are turned on so as to increase a potential of the substrate. If the potential of the substrate becomes high, a voltage drop (for example, 0.7V) occurs with ease between the source of the bipolar transistor B1 and substrate. Thus, the triggering voltage of the bipolar transistor B1 is reduced.

[0029] As a result, a triggering of the bipolar transistor B1 may occur even at a low voltage. If the bipolar transistor B1 is turned on at the low voltage, a voltage applied to the NMOS transistor N1 and its gate insulating layer is reduced. Thus, the influence or damage to the gate insulating layer of the NMOS transistor N1 is decreased.

[0030] Moreover, when measured by applying a voltage to the substrate of the NMOS transistor N1 in the manner of the present invention, a second breakdown current (It2 value) representing ESD performance becomes even higher.

[0031] As mentioned in the above description, the present invention improves ESD performance by turning on the parasitic bipolar transistor of the NMOS transistor at a voltage lower than that of the conventional art.

[0032] Accordingly, the present invention allows the prevention of a gate insulating layer from receiving a high voltage by turning on a protection circuit at a lower

voltage so as to shunt the ESD current as well as improve ESD performance by increasing a magnitude of It2.

[0033] The invention being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.